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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,560	01/16/2001	Kenny Kok-Hoong Chiu	052404.0098	3810

7590 05/18/2005

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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,560	CHIU, KENNY KOK-HOONG	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 10 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14,17-22,24-28,30,32-36 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-14,17-22, 24-28, 30, 32-35 and 36* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 10-12, 24-26 and 38 is withdrawn in view of the newly discovered reference(s) to Stachura et al. (US Patent 6,292,038 B1). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4-12, 28, 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Stachura et al. (US Patent 6,292,038 B1).

(1) With regard to claim 1, Stachura et al t discloses in Fig. 3, a clock selection device adapted to select one of a pair of clock sources onto an output clock line, comprising: a first input clock line (310) coupled to a first clock source (CLK A); a second input clock line (320) coupled to a second clock source (CLK B), the second clock source asynchronous to the first clock source (col. 3, line 66 - col. 4, line 4); and a clock selection logic (multiplexers of both circuits) adapted to select from the first input clock line and the second input clock line, producing an internal clock line coupled to the output clock line (col. 6, lines 47-63); and a clock

synchronization logic (SEL A_SYNC, SEL B_SYNC) coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 3, lines 5-13) wherein the clock synchronization logic is independent of the internal clock line (Fig. 3 shows the clock synchronization logic, independent of the internal clock line) wherein the first clock source has a first frequency, and wherein the second clock source has a second frequency, the second frequency independent of the first frequency (col. 2, lines 19-25; claim 1).

(2) With regard to claim 4, Stachura et al. also discloses the clock selection device of claim 1, the clock synchronization logic comprising: a first clock synchronization block (SEL A_SYNC), coupled to the first clock source (CLK A), adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block (SEL B_SYNC), coupled to the second clock source (CLK B), adapted to synchronize the second clock source and the clock selection logic.

(3) With regard to claim 5, Stachura et al. also discloses the clock synchronization logic further comprising: a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 4, lines 27-40).

(5) With regard to claim 6, Stachura et al. also teaches the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 3, lines 51-65).

(6) With regard to claim 7, Stachura et al. also teaches in Fig. 3, wherein the clock selection logic comprises a multiplexer with two clock input lines.

(7) With regard to claim 8, Stachura et al. also teaches wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level (col. 4, lines 27-lines 61).

(8) With regard to claim 9, Stachura et al. also teaches the clock selection device of claim 1, further comprising: a clock selection signal, asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is deasserted (col. 4, lines 27-lines 61).

(9) With regard to claims 10-12, though Stachura et al. does not explicitly teach the exact configurations of the clock selecting device, Stachura et al. does however does teach that multiple configurations of the circuitry may be used. Therefore, the configurations taught by applicant in claims 10-12 would merely be a design choice to accomplish the same results as Stachura et al., i.e. Glitch-free clock selection.

(10) With regard to claim 28, claim 28 inherits all limitations of claim 1, above as claim 28 merely cites the method of the clock selection device of claim 1.

(11) With regard to claim 32, Stachura et al. also discloses the step of synchronizing comprising the step of: delaying step (c) for a predetermined amount of time (Fig. 3, SEL B_DELAY; col. 3, lines 32-50).

(12) With regard to claim 33, Stachura et al. also discloses With discloses resetting a synchronization logic with a first reset signal synchronous to the first clock signal; and resetting the synchronization logic with a second reset signal synchronous to the second clock signal (Fig. 4, col. 4, lines 27-40).

(13) With regard to claim 34, Stachura et al. also discloses the method of claim 28, step (c) comprising the steps of receiving a clock select signal asynchronous to the first clock signal and the second clock signal; and connecting the first clock signal to the output clock line when the clock select signal is asserted; connecting the second clock signal to the output clock line when the clock select signal is deasserted; synchronizing the first input clock signal, the second input clock signal, and steps) and, such that the output clock line is glitch free (Fig.. 3; col. 4, lines 27-50).

(14) With regard to claim 35, claim 35 inherits all limitations of claim 1 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13, 14, 17-22, 24-27, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stachura et al. (US Patent 6,292,038) as applied to claims 1, 28, and 35 above, in view of Iknaian et al. (US Patent 5,294,842).

(1) With regard to claim 13, Stachura et al. discloses all limitations of claim 1, above. Stachura et al. does not however disclose the clock selection device further comprising: a buffer coupled to the internal clock line, producing a buffered output clock signal.

However, Iknaian et al. discloses in Fig. 5, a clock selection device further comprising: a buffer coupled to an internal clock line, producing a buffered output clock signal.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Iknaian et al. with those of Stachura et al. as a method of distributing the clock signals to other circuitry.

(2) With regard to claim 14, as noted above, Stachura et al. discloses all limitations of the clock selection device as disclosed in claim 1 and 14. Furthermore, Iknaian et al's invention relates to synchronization of clock signals in a computer system. Therefore, a processor would be obvious as would be the use of the synchronization device throughout the computer system through a plurality of communication controllers to incorporate its benefits throughout the system.

(3) With regard to claim 17, Stachura et al. also discloses the processor device of claim 14, the clock synchronization logic comprising: a first clock synchronization block (SEL A_SYNC), coupled to the first clock source (CLK A), adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block (SEL B_SYNC),

coupled to the second clock source (CLK B), adapted to synchronize the second clock source and the clock selection logic.

(4) With regard to claim 18, Stachura et al. also discloses the clock synchronization logic further comprising: a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 4, lines 27-40).

(5) With regard to claim 19, Stachura et al. also teaches wherein the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 3, lines 51-65).

(6) With regard to claim 20, Stachura et al. also teaches in Fig. 3, wherein the clock selection logic comprises a multiplexer with two clock input lines.

(7) With regard to claim 21, Stachura et al. also teaches wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level (col. 4, lines 27-lines 61).

(8) With regard to claim 22, Stachura et al. also teaches the clock selection device of claim 1, further comprising: a clock selection signal, asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first

input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is deasserted (col. 4, lines 27-lines 61).

(9) With regard to claims 24-26, though Stachura et al. does not explicitly teach the exact configurations of the clock selecting device, Stachura et al. does however does teach that multiple configurations of the circuitry may be used. Therefore, the configurations taught by applicant in claims 24-26 would merely be a design choice to accomplish the same results as Stachura et al., i.e. Glitch-free clock selection.

(10) With regard to claim 27, Iknaian et al. also discloses in Fig. 5, a clock selection device further comprising: a buffer coupled to an internal clock line, producing a buffered output clock signal.

(11) With regard to claim 30, claim 30 inherits all limitations of claim 28 above. Furthermore, Iknaian et al. discloses the method of claim 28 further comprising the steps of: buffering the internal clock line to generate the output clock line.

6. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stachura et al. (US Patent 6,292,038) as applied to claim 35 above, in view of Watt (US Patent 5,675,615).

As noted above, Stachura et al. discloses all limitations of claim 35. Stachura et al. does not explicitly disclose the clock synchronization logic further comprising: a first reset means synchronized to the first clock source for resetting the clock synchronization means; and a second means, synchronized to the second clock source for resetting the clock synchronization means, wherein the first reset means and the second reset means signal can prevent meta-stability

of the clock synchronization means, though Stachura et al. teach the use of an auxiliary reset (Fig. 4, col. 4, lines 27-40).

However, Watt teaches in Fig. 5, the clock synchronization logic further comprising: a first reset means (36) synchronized to the first clock source for resetting the clock synchronization means; and a second means (reset), synchronized to the second clock source for resetting the clock synchronization means, wherein the first reset means and the second reset means signal can prevent meta-stability of the clock synchronization means (col. 7, lines 7-23).

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the teachings of Watt into the invention of Stachura et al. as a known method of clock switching and synchronizing (abstract).

Allowable Subject Matter

7. Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a clock switching technique and mechanism. A search of prior art records failed to teach a mechanism comprising: " a first feedback means coupled to the clock selection means and the first synchronization means for synchronizing the second synchronization means and the clock selection means; and a second feedback means coupled to

the clock selection means and the second synchronization means for synchronizing the first synchronization means and the clock selection means" as disclosed in claim 38.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
May 10, 2005

AMANDA T. LE
PRIMARY EXAMINER